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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/777,368
Filing Date: February 12, 2004
Appellant(s): RITZ ET AL.

Himanshu S. Amin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06/02/2008 appealing from the Office action mailed 04/03/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US Publication 2004/0193755	Safranek et al.	09-2004
US Patent 6,922,740	Kondratiev et al.	07-2005

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-5, 7-17 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Safranek et al. (US Pub 2004/0193755) in view of Kondratiev et al. (US Patent 6,922,740).

2. As per claim 1, Safranek teaches a direct memory access memory corruption detection system embodied on a computer readable medium comprising the following computer executable components:

an access data store that stores access information (e.g. access information stored in NoDMA table 103 and NoDMA cache 109 of Fig 1) associated with memory (Fig. 1, ref. 101), the access data store comprising an access table (Fig. 1, ref. 103 and Fig. 3), the access table comprising an access attribute field, the access attribute field distinguishes no access to indicate no access ([0011]-[0021]; [0034] and [0038]); and

a memory controller (Fig. 1, ref. 117) that employs the access information to determine whether a requested direct memory access is permitted and rejects the requested direct memory access if it is not permitted (Fig. 4, ref. 417) and allows the

requested direct memory access if it is permitted (Fig. 4, ref. 419) ([0014]-[0021]; [0034] and [0038]).

Safranek does not teach the computer readable medium comprising: a source identifier field and a memory address field; distinguishing between read, read and write, and write ... ; and a combination of source associated with the access attribute ... .

Kondratiev teaches a system and a method comprising:

an access information comprising a source identifier field (e.g. device ID) and a memory address field (e.g. read access with memory address range, write access with memory address range) (Fig. 2, ref. 210 and col. 4, ll. 40-65); and

an access attribute distinguishing between read, read and write and write to indicate read, read and write or write for a combination of source associated with the access attribute and memory address range associated with the access attribute identified in the source identifier field (e.g. device ID) and memory address field (Fig. 2, ref. 210 and col. 4, ll. 40-65).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kondratiev's device ID, and read and write access attribute with memory address range into Safranek's DMA memory corruption detection system for the benefit of increase security and reliability for accessing DMA (Kondratiev, col. 7, ll. 30-41) to obtain the invention as specified in claim 1.

3. As per claims 2-3, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Kondratiev further teaches the direct memory access memory

corruption detection system comprising the access information comprising a direct memory access request, and wherein the direct memory access request comprising a transaction type (e.g. read-write access) (Kondratiev, Fig. 2 and col. 4, ll. 23-26).

4. As per claims 4-5, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Kondratiev further teaches the direct memory access memory corruption detection system comprising the direct memory access request comprising a source identifier (e.g. device ID), and wherein the source identifier being associated with a device (I/O device 140-1 of Fig. 1 and device ID of Fig. 2) (Kondratiev, col. 4, ll. 40-65).

5. As per claim 7, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the access information comprising at least one permitted memory address (Safranek, [0014] and [0021]), wherein certain segments of the memory do not have access restriction, therefore request for access are allowed.

6. As per claim 8, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the access information comprising at least one disallowed memory address (Safranek, [0014] and [0021]), wherein certain

segments of the memory have access restriction, therefore request for access are denied.

7. As per claim 9, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the request comprising a read action or a write action (Safranek, [0015]).

8. As per claim 10, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the request comprising a peripheral component interface express bus transaction (Safranek, [0017] and [0019]).

9. As per claim 11, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the memory controller coupled to a device through a peripheral component interface express bus, the device providing the request (Safranek, [0017] and [0019]).

10. As per claim 12, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the memory controller further providing

error information, if the requested direct memory access is not permitted (Safranek, Fig. 4; [0034] and [0038]), wherein the error is logged and can be utilized for subsequent analyzing.

11. As per claim 13, Safranek and Kondratiev teach all the limitation of claim 12 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising the error information comprising source information associated with the requested direct memory access (Safranek, Fig. 4; [0034] and [0038]).

12. As per claim 14, Safranek teaches a direct memory access memory corruption detection system embodied on a computer readable medium comprising the following computer executable components:

a memory controller (Fig. 1, ref. 117) that includes an access data store comprising an access table (Fig. 1, ref. 103, 109 and Fig. 3), the access table comprising an access attribute field, the access attribute field contains an access attribute that distinguishes no access to indicate no access, wherein the access attribute contains data indicating no access when the access attribute is not permitted access to a memory page associated with the access attribute (Fig. 4; [0011]-[0021]; [0034] and [0038]); and

the memory controller (Fig. 1, ref. 117) employs the access information to determine whether a requested direct memory access is permitted and rejects the

requested direct memory access if it is not permitted (Fig. 4, ref. 417) and allows the requested direct memory access if it is permitted (Fig. 4, ref. 419) ([0014]-[0021]; [0034] and [0038]).

Safranek does not teach the computer readable medium comprising: a source identifier field and a memory address field; distinguishing between read, read and write, and write, to indicate read, read and write, and write ... , wherein the access attribute contains data indicating read ..., wherein the access attribute contains data indicating write ..., wherein the access attribute contains data indicating read and write ... ; and a device driver ... .

Kondratiev teaches a system and a method comprising:

an access information comprising a source identifier field (e.g. device ID) and a memory address field (e.g. read access with memory address range, write access with memory address range) (Fig. 2, ref. 210 and col. 4, ll. 40-65);

an access attribute distinguishing between read, read and write and write to indicate read, read and write or write for a combination of source associated with the access attribute and memory address range associated with the access attribute identified in the source identifier field (e.g. device ID) and memory address field (Fig. 2, ref. 210 and col. 4, ll. 40-65);

wherein the access attribute contains data indicating read when the source identified by the source identifier associated with the access attribute is only permitted to read the memory address range associated with the access attribute (Fig. 2, ref. 210 and col. 4, ll. 40-65), as the access attribute provide only read access range,

wherein the access attribute contains data indicating write when the source identified by the source identifier associated with the access attribute is only permitted to write to the memory address range associated with the access attribute (Fig. 2, ref. 210 and col. 4, ll. 40-65), as the access attribute provide only write access range,

wherein the access attribute contains data indicating read and write when the source identified by the source identifier associated with the access attribute is permitted to read and write to the memory address range associated with the access attribute (Fig. 2, ref. 210 and col. 4, ll. 40-65), as the access attribute provide read and write access range; and

a device driver (e.g. bus master) that programs (e.g. program by invoking a function to request DMA access) a device for a direct memory access operation, and provides the access information to the memory controller via a direct memory access application interface (col. 4, ll. 6-26 and col. 6, ll. 43-53).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kondratiev's device ID, read and write access attribute with memory address range and the bus master into Safranek's DMA memory corruption detection system, wherein the combination of Safranek and Kondratiev further teaches:

wherein the source identified by the source identifier associated with the access attribute is not permitted access to the memory address range associated with the access attribute (Safranek, Fig. 4; [0011]-[0021]; [0034]; [0038] and Kondratiev, Fig. 2, ref. 210 and col. 4, ll. 40-65),

for the benefit of increase security and reliability for accessing DMA (Kondratiev, col. 7, ll. 30-41) to obtain the invention as specified in claim 14.

13. As per claim 15, Safranek and Kondratiev teach all the limitations of claim 14 as discussed above, where Kondratiev further teaches the direct memory access memory corruption detection system further comprising the stored access information comprising a range of physical memory (access range), a source identifier (device ID), and an access attribute (read and write) (Kondratiev, Fig. 2).

14. As per claim 16, Safranek and Kondratiev teach all the limitations of claim 14 as discussed above, where Safranek teaches the direct memory access memory corruption detection system comprising wherein the request comprising a peripheral component interface express bus transaction (Safranek, [0017] and [0019]).

15. As per claim 17, Safranek teaches a method that facilitates detection of direct memory access memory corruption comprising:

receiving a request for a direct memory access transaction, the request comprising a least one memory address ([0014]-[0021] and [0034]);

determining whether the request is permitted based, at least in part on, stored access information (Fig. 1, ref. 103, 109 and Fig. 3) and the request, the stored access information comprising at least one access attribute, an access attribute distinguishes no access to indicate no access (Fig. 4; [0011]-[0021]; [0034] and [0038]); and

rejecting the requested direct memory access if it is not permitted (Fig. 4, ref. 417) and allowing the direct memory access if it is permitted (Fig. 4, ref. 419) ([0014]-[0021]; [0034] and [0038]).

Safranek does not teach the method comprising: the request comprising a source identifier, and an access attribute; at least one source identifier and at least one memory address range; and distinguishes between read, read and write, and write to indicate read, read and write, or write … .

Kondratiev teaches a system and a method comprising:

a request including a source identifier (e.g. device ID), and an access attribute (e.g. read, write) (Fig. 2 and col. 3, l. 51 to col. 4, l. 65);

an access information comprising at least one source identifier (e.g. device ID) and at least one memory address range (e.g. read access with memory address range, write access with memory address range) (Fig. 2, ref. 210 and col. 4, ll. 40-65); and

an access attribute distinguishing between read, read and write and write to indicate read, read and write or write for a combination of source associated with the access attribute and memory range associated with the access attribute identified by the at least one source identifier and at least one memory address range (Fig. 2, ref. 210 and col. 4, ll. 40-65).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kondratiev's device ID, read and write access attribute with memory address range and the bus master into Safranek's DMA memory corruption detection system for the benefit of increase security and reliability for

accessing DMA (Kondratiev, col. 7, ll. 30-41) to obtain the invention as specified in claim 17.

16. As per claim 19, Safranek and Kondratiev teach all the limitations of claim 17 as discussed above, where Kondratiev further teaches the method that facilitates detection of direct memory access memory corruption comprising storing access information in an access data store, the access information comprising a source identifier (device ID), at least one memory address (access range) and an access attribute (read and write) (Kondratiev, ACL 210 Fig. 2).

17. As per claim 20, Safranek and Kondratiev teach all the limitations of claim 17 as discussed above, where Safranek further teaches the method that facilitates detection of direct memory access memory corruption comprising a computer readable medium having stored thereon computer executable instructions for carrying out the method (Safranek, [0039]).

18. As per claim 21, Safranek teaches a data packet transmitted between two or more components embodied on a computer readable medium that facilitates detection of direct memory access memory corruption, the data packet comprising:

a data field comprising a corrected platform error event ([0034] and [0038]), the corrected platform error event being based, at least in part, upon a determination that a requested direct memory access is not permitted ([0034] and [0038]), the determination

being based, at least in part, upon access information stored in an access table (Fig. 1, ref. 103, 109 and Fig. 3) and the requested direct memory access (Fig. 4; [0011]-[0021]; [0034] and [0038]), the access information comprising at least one access attribute, the at least one access attribute distinguishes no access to indicate no access (Fig. 4; [0011]-[0021]; [0034] and [0038]).

Safranek does not teach the system comprising: at least one source identifier and at least one memory address range; and distinguishing from amongst read, read and write, and write to indicate read, read and write, or write … .

Kondratiev teaches a system and a method comprising:

an access information comprising at least one source identifier (e.g. device ID) and at least one memory address range (e.g. read access with memory address range, write access with memory address range) (Fig. 2, ref. 210 and col. 4, ll. 40-65); and

an access attribute distinguishes from amongst read, read and write, and write to indicate read, read and write, or write for a combination of source and memory address range identified by the at least one source identifier and at least one memory address range associated with the at least one access attribute (Fig. 2, ref. 210 and col. 4, ll. 40-65).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kondratiev's device ID, and read and write access attribute with memory address range into Safranek's DMA memory corruption detection system for the benefit of increase security and reliability for accessing DMA (Kondratiev, col. 7, ll. 30-41) to obtain the invention as specified in claim 21.

19. As per claim 22, Safranek teaches a direct memory access memory corruption detection system embodied on a computer readable medium comprising:

means for storing access information (Fig. 1, ref. 103, 109 and Fig. 3) associated with memory (Fig. 1, ref. 101) ([0011]-[0021]);

means for receiving a request for a direct memory access ([0014]-[0021] and [0034]);

means for determining whether a requested direct memory access is permitted based, at least in part, upon the stored access information and the request, the stored access information comprising at least one access attribute, the at least one access attribute distinguishes no access to indicate no access (Fig. 4; [0011]-[0021]; [0034]) and [0038]); and,

means for rejecting the requested direct memory access if it is not permitted (Fig. 4, ref. 417) and allowing the direct memory access if it is permitted (Fig. 4, ref. 419) ([0014]-[0021]; [0034] and [0038]).

Safranek does not teach the system comprising: at least one source identifier and at least one memory address range; and distinguishes between read, read and write, and write to indicate one of read, read and write, or write ... .

Kondratiev teaches a system and a method comprising:

an access information comprising at least one source identifier (e.g. device ID) and at least one memory address range (e.g. read access with memory address range, write access with memory address range) (Fig. 2, ref. 210 and col. 4, ll. 40-65); and

an access attribute distinguishes between read, read and write, and write to indicate one of read, read and write, or write for a combination of source and memory address range identified by the at least one source identifier and at least one memory address range associated with the at least one access attribute (Fig. 2, ref. 210 and col. 4, ll. 40-65).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kondratiev's device ID, and read and write access attribute with memory address range into Safranek's DMA memory corruption detection system for the benefit of increase security and reliability for accessing DMA (Kondratiev, col. 7, ll. 30-41) to obtain the invention as specified in claim 22.

(10) Response to Argument

I. claims 1-5 and 7-13

Issue I

Appellant seems to argue (on page 6) that the combination of the references improper because of hindsight.

Examiner's response to Issue

In response to appellant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed

invention was made, and does not include knowledge gleaned only from the appellant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Furthermore, the examiner respectfully disagrees appellant's above arguments for the following reasoning:

Safranek teaches accessing of data via direct memory access (DMA) comprising an access table having an access attribute, associated with a memory, with no access information to indicate no access.

Safranek does not teach the access table comprising a source identifier field and a memory address field, and wherein the access attribute distinguishing between read, read and write, and write to indicate read, read and write, or write for a combination of source associated with the access attribute and memory range address associated with the access attribute identified in the source identifier field and memory address field.

Kondratiev teaches access of data via DMA comprising an access table having a source identifier field, a memory address field and an access attribute field, the access attrite field distinguishes between read, read and write, and write to indicate read, read and write, write for a combination of source associated with the access attribute and memory range address associated with the access attribute identified in the source identifier field and memory address field, and further discloses that Kondratiev's source identifier field, memory address field

and access attribute field increase the security and reliability for DMA data accessing.

It would have been obvious to one having skilled in the art in controlling DMA data accessing to include the source identifier field, the memory address field, and the access attribute field distinguishes between read, read and write, and write disclosed by Kondratiev into the access table of Safranek to achieve the claimed invention. As disclosed in Kondratiev, the motivation for the combination would be to increase the security and reliability for DMA data accessing.

Issue II

Appellant argued (on pages 6-7) that the combination of Safranek and Kondratiev do not teach appellant's invention as recited in the subject claims because Safranek lack the combined source, memory and access type control and Kondratiev's table only indicates memory ranges that are allowed access and does not provide the ability to directly specify a memory range that is not allowed access.

Examiner's response to Issue

In response to appellant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642

F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Additionally, the examiner respectfully disagrees appellant's above arguments because the examiner relied on the combination of Safranek and Kondratiev for the teaching of the subject claims as following: Safranek teaches a table indicating memory access that is not allowed, and Kondratiev teaches a table with the combined source, memory, and access type control that is allowed; therefore, the resulting combination of the references further teaches the table with the combined source, memory, and access type control that is allowed and not allowed; furthermore, it is advantageous to combine Kondratiev's control parameters that is allowed into Safranek's table with control parameter that is not allowed for the benefit of increasing the security and reliability for data accessing.

Issue III

Appellant argued (on page 7) that the combination of Safranek and Kondratiev do not teach appellant's invention as recited in the subject claims because Safranek's read and write access are indicated in two separate fields by specifying a memory address in each of the two separate read memory range and write memory range, where as the claimed access attribute field is within a single field having indication that distinguished between allowed and disallowed access information.

Examiner's response to Issue

In response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which appellant relies (i.e., single access attribute field) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, the examiner respectfully disagrees appellant's above arguments because in according to the Specification cited by the appellant (i.e. page 7, lines 6-9 and page 8, lines 8-22) and also according to the appellant's explanation during the interview dated 02/22/2008, it is the examiner's understanding that the field is singular because the information associated with the field is located within a single column (Drawings, Figure 3), without specific disclosure as to how data are structured within the single column; therefore, Kondratiev does teach the single field of access control list (ACL) (Fig. 2, ref. 210) having a plurality of sub-fields/sub-data, as the field of ACL is within a single column; or one skilled in the art views the combined sub-fields/sub-data of read access range and write access range to be the singular column.

Issue IV

With regard to the appellant's example and statement (on page 7) that by using the combination of the plurality of fields, memory access privileges can be defined using reduced table space.

Examiner's response to Issue

It is not fully clear to the examiner, in view of appellant's citation associated with the claimed limitation (i.e. page 7, lines 6-9 and page 8, lines 8-22), where in the Specification or Drawings disclose that the table space is reduced. Furthermore, considering the claimed invention's field being singular is supported/enabled by having the information associated with the field located within the single column (i.e. page 7, lines 6-9 and page 8, lines 8-22), and there seems to have no specific disclosure as to exactly the amount of data contained within the single column; therefore, without providing a numerical value associated with the data contained within the single column for comparison, the examiner is not clear as to how the appellant came to the resulting conclusion that the table space is reduced.

II. claims 14-16

Issue I

Appellant presented arguments (on pages 9-10) similar to those presented for claims 1-5 and 7-13 above.

Examiner's response to Issue

The examiner will apply the same response for each of the arguments presented above for claims 1-5 and 7-13 towards claims 14-16 respectively.

Issue II

Appellant presented arguments (on page 10) that the combination of references would not result in the claimed invention because resulting combination of references provide less control for memory access and require more data table space.

Examiner's response to Issue

The examiner respectfully disagrees, the examiner is not fully clear as to how the resulting combination of the references would provide less control for memory access considering the combination of references results in all the fields with the corresponding control by a memory controller claimed by the appellant, and the examiner is also not fully clear as to appellant's resulting conclusion that the combination of references would require more table space, considering the claimed invention's field being singular is supported/enabled by having the information associated with the field located within a single column (i.e. page 7, lines 6-9 and page 8, lines 8-22), and there seems to have no specific disclosure as to exactly the amount of data contained within the single column; therefore, without providing a numerical value associated with the data contained within the single column for comparison, the examiner is not clear as to how the comparison can be made between the claimed invention and the combination of references.

III. claims 17, 19 and 20

Issue

Appellant presented arguments (on pages 10-12) similar to those presented for claims 1-5 and 7-13 above.

Examiner's response to Issue

The examiner will apply the same response for each of the arguments presented above for claims 1-5 and 7-13 towards claims 17, 19 and 20 respectively.

IV. claim 21

Issue I

Appellant presented arguments (on pages 12-13) similar to those presented for claims 1-5 and 7-13 above.

Examiner's response to Issue

The examiner will apply the same response for each of the arguments presented above for claims 1-5 and 7-13 towards claim 21 respectively.

V. claim 22

Issue I

Appellant presented arguments (on pages 13-15) similar to those presented for claims 1-5 and 7-13 above.

Examiner's response to Issue

The examiner will apply the same response for each of the arguments presented above for claims 1-5 and 7-13 towards claim 22 respectively.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Chun-Kuan Lee
Patent Examiner
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